REMARKS

By this amendment, claims 1, 3, 6, 10, 20, 22, 26, 28, 30-31, and 36 have been amended. Claims 1, 3-20, 22-31, and 33-36 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

On August 23, 2006, Applicants' representative conducted a telephonic interview with the Examiner. The following amendment substantially addresses those issues discussed in relationship to prior art (Pain et al., Yang et al.) rejections. Agreement with respect to claims 1 and 20 was reached.

Claims 22 and 36 have been amended in minor fashion and are now in condition for allowance.

Claims 3, 26, 28, and 30 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims have been amended to address the concerns raised in the Office Action. Applicant respectfully requests that the rejection of these claims be withdrawn and the claims allowed.

Claims 20, 26-29, and 31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Pain et al. (US WO 99/48281). This rejection is respectfully traversed.

Claims 20 and 31, as amended, recite a charge-domain readout circuit comprising, *inter alia*, "a plurality of column readout circuits ..., wherein each column readout circuit is associated with a respective column of sensors ..., each of said plurality of column readout circuits comprising: a first plurality of charge storage devices for storing each of said multiple pixel signal values from said column of sensors, [and] a second plurality of charge storage devices for storing each of said

multiple reset signal values from said column of sensors" (emphasis added). Claim 26, as amended, recites a method of reading out values from active pixel sensors comprising, *inter alia*, "selecting multiple rows of sensors ... on a column line; storing correlated double sampled values for a plurality of sensors in said selected rows on the column line, wherein said values for each sensor are stored by a respective pair of charge storage devices in a readout circuit associated with a column in said array in which said sensor is located; [and] combining said stored signal values" (emphasis added). Applicant respectfully submits that Pain et al. does not disclose these limitations.

To the contrary, Pain et al. discloses only capacitor CIS which combines pixel signals, and capacitor CIR which combines reset signals, but does not disclose storing multiple signal values, then combining the separate stored signal values and outputting them. Pain et al. FIG. 2A. Applicant respectfully submit that Pain et al. does not disclose, teach, or suggest a plurality of column readout circuits comprising first plurality of charge storage devices for respectively storing each of said multiple pixel signal values and a second plurality of charge storage devices for respectively storing each of said multiple reset signal values as recited in claims 20 and 31. Furthermore, Applicant respectfully submits that Pain et al. does not disclose, teach, or suggest storing correlated double sampled values for a plurality of sensors by a respective pair of charge storage devices and combining said stored signal values as recited in claim 26.

Since Pain et al. does not disclose all the limitations of claims 20 and 31, claims 20 and 31 are not anticipated by Pain et al. Claims 27-29 depend from claim 26 and are patentable at least for the reasons mentioned above, and on their own merits. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection be withdrawn and claims 20, 26-29, and 31 be allowed.

Claims 1, 3-13, 18, 20, 22, 24, 31, and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Yang et al. (US 2004/0246354). This rejection is respectfully traversed.

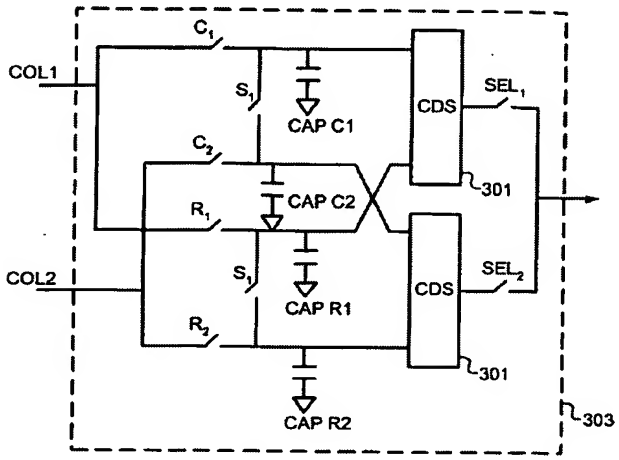
Claim 1, as amended, recites an image sensor readout circuit comprising, *inter alia*, "a binning circuit coupled to said column line, wherein said binning circuit comprises: a first plurality of charge storage devices for respectively storing a predetermined first plurality of analog pixel signal values from a plurality of pixels from said column line, [and] a second plurality of charge storage devices for respectively storing a predetermined second plurality of analog reset signal values from said plurality of pixels from said column line" (emphasis added). Claim 6, as amended, recites a binning circuit comprising, *inter alia*, a "a column line for receiving analog pixel and analog reset signal values of an active pixel sensor; a first sample circuit coupled to said column line, said first sample circuit comprising a first plurality of charge storage devices respectively storing a first plurality of analog pixel signal values from a plurality of pixels from said column line; [and] a second sample circuit coupled to said column line, said second sample circuit comprising a second plurality of charge storage devices respectively storing a second plurality of analog reset signal values from said plurality of pixels from said column line" (emphasis added). Applicant respectfully submits that Yang et al. does not disclose these limitations.

Claim 10, as amended, recites a method of binning the output of an active image sensor comprising, *inter alia*, "sampling and respectively storing analog output signal values from a plurality of pixels from a column line ...; sampling and respectively storing analog reset signal values from said plurality of pixels from said column line ...; subsequently combining and outputting all sampled and stored analog output signal values ...; and combining and outputting all sampled and stored analog reset signal values" (emphasis added). Claims 20 and 31 recite a charge-domain readout circuit

comprising, *inter alia*, "a plurality of column readout circuits ..., wherein each column readout circuit is associated with a respective column of sensors in said active pixel sensor, each of said plurality of column readout circuits comprising: a first plurality of charge storage devices for respectively storing each of said multiple pixel signal values from said column of sensors, a second plurality of charge storage devices for respectively storing each of said multiple reset signal values from said column of sensors" (emphasis added). Applicant respectfully submits that Yang et al. does not disclose these limitations.

To the contrary, Yang et al. discloses two separate column lines, COL1 and COL2, each of which has a single capacitor for storing a pixel signal and a single capacitor for storing a reset signal. FIG. 2 (reproduced below). There is no first and second plurality of charge storage devices coupled to the same column line. Applicant respectfully submits that Yang et al. does not disclose, teach, or suggest "a binning circuit coupled to said column line, wherein said binning circuit comprises: a first plurality of charge storage devices for respectively storing a predetermined first plurality of analog pixel signal values ... from said column line, and a second plurality of charge storage devices for respectively storing a predetermined second plurality of analog reset signal values ... from said column line," as recited in claim 1.

Yang et al. FIG. 2



Nor does Yang et al. teach a column line, first and second sample circuits coupled to said column line, respectively comprising first and second pluralities of charge storage devices respectively storing a first plurality of analog pixel signal values and a second plurality of analog reset signal values from a plurality of pixels from said column line as recited in claim 6. Yang et al. also does not teach "sampling and respectively storing analog output signal values from a plurality of pixels from a column line; [and] sampling and respectively storing analog reset signal values from said plurality of pixels from said column line," as recited in claim 10. Furthermore, Yang et al. does not teach that "each column readout circuit is associated with a respective column of sensors ..., each of said plurality of column readout circuits comprising: a first plurality of charge storage devices for respectively storing each of said multiple pixel signal values from said column of sensors, a second plurality of charge storage devices for respectively storing each of said multiple reset signal values from said column of sensors," as recited in claims 20 and 31.

Since Yang et al. does not disclose all the limitations of claims 1, 6, 10, 20, and 31, claims 1, 6, 10, 20, and 31 are not anticipated by Yang et al. Claims 3-5, 7-9, 11-13, 18, 22, 24, and 33 depend, respectively, from claims 1, 6, 10, 20, and 31, and are patentable

at least for the reasons mentioned above, and on their own merits. Applicant respectfully requests that the 35 U.S.C. § 102(e) rejection of claims 1, 3-13, 18, 20, 22, 24, 31, and 33 be withdrawn and the claims allowed.

Claims 14-17 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang et al in view of Funakoshi et al (US 2002/0154347). This rejection is respectfully traversed. Claims 14-17 and 19 depend from claim 10 and are patentable at least for the reasons mentioned above, and on their own merits. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 14-17 and 19 be withdrawn and the claims allowed.

Claims 23, 26-30, and 34-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang et al. in view of Applicant's Admitted Prior Art (AAPA). This rejection is respectfully traversed.

Claims 23 and 34-36 depend, respectively, from claims 20 and 31, and are patentable at least for the reasons mentioned above, and on their own merits.

In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Neither Yang et al. nor AAPA, even when considered in combination, teach or suggest all limitations of independent claim 26.

Claim 26 recites a method of reading out values from active pixel sensors comprising, *inter alia*, "selecting multiple rows of sensors ... on a column line; storing correlated double sampled values for a plurality of sensors in said selected rows on the column line, wherein said values for each sensor are stored by a respective pair of charge storage devices in a readout circuit associated with a column in said array in

which said sensor is located; [and] combining said stored signal values" (emphasis added). Yang et al. does not teach or suggest these limitations.

To the contrary, as discussed above, Yang et al. teaches two separate column lines, COL1 and COL2, each of which has a single capacitor for storing a pixel signal and a single capacitor for storing a reset signal. FIG. 2 (reproduced below). There is no first and second plurality of charge storage devices coupled to the same column line. Applicant respectfully submits that Yang et al. does not disclose, teach, or suggest that values for each sensor are stored by a respective pair of charge storage devices in a readout circuit associated with a column as recited in claim 26. Nor is AAPA cited for this limitation. Thus, AAPA does not remedy the deficiency of Yang et al.

Since Yang et al. and AAPA do not teach or suggest all of the limitations of claim 26, claim 26 and dependent claims 27-30 are not obvious over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 23, 26-30, and 34-36 be withdrawn and the claims allowed.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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